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Breaking Barriers For Next Generation Wireless Chips

ScienceDaily (Nov. 4, 2008) — The Mathematical Institute of the University of Cologne conducts research within in the European project ICESTARS (Integrated Circuit/Electromagnetic Simulation and design Technologies for Advanced Radio Systems-on-chip). New mathematical algorithms for the next radio chip generation will be developed under the leadership of Prof. Dr. Caren Tischendorf.

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According to Prof. Tischendorf: "In the future, mobile devices will provide customers with services ranging from telephony and internet to mobile TV and remote banking, anytime, anywhere. It is impossible to realize the necessary, extremely high data transfer rates within the frequency bands used today (approximately 1-3GHz)." The project serves to enable the development of low-cost wireless chips that can operate in a frequency range of up to 100GHz.

The leader of the ICESTARS project, Marq Kole of NXP Semiconductors says: "By the end of the project in 2010 we aim to have accelerated the chip

development process in the extremely high frequency range by new methods and simulation tools in order to actively maintain the European chip developers on a top position over the whole spectrum of wireless communications." The ICESTARS project is funded by the European Commission within the EU 7th framework program and lead by Dutch company NXP Semiconductors. The German semiconductor company Qimonda will develop advanced analog simulation techniques in the framework of this project.

Additional partners are the software developing companies AWR-APLAC from Finland with a focus onto frequency-domain simulation algorithms and MAGWEL from Belgium with a focus onto electromagnetic simulations. Besides the University of Cologne, the university partners Upper Austria University of Applied Sciences, the University of Wuppertal from Germany and the University of Oulu from Finland are concentrating on modeling questions, algorithmic problems and simulation issues to be solved for a robust and accelerated automated testing of analog circuits with digital signal processing in the extremely high frequency range.

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