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European Research Collaboration to Break Barriers for Next-generation Wireless Chips

Tues. November 4, 2008

Source: AWR

AWR, a leader in high-frequency electronic design automation (EDA), announced that its Finnish R&D facility will conduct research within the European Integrated Circuit/Electromagnetic Simulation and design Technologies for Advanced Radio [Systems](#)-on-chip (ICESTARS) project. ICESTARS strives to enable the development of low-cost wireless chips that can operate at frequencies up to 100 GHz.

"With mobile device services such as Internet access, mobile TV and remote banking becoming mainstream, very high data transfer rates are a must," said Taisto Tinttunen, R&D director of AWR-APLAC Corp. "Consequently, there is a growing demand for simulation technologies that not only address these fast data transfer rates, but also scale well beyond current frequencies used for wireless communications." AWR's efforts within the scope of ICESTARS will focus on frequency-domain simulation methods for next-generation wireless system on chip (SoC) devices, and will be led by Tinttunen.

The leader of the ICESTARS project, Marq Kole of NXP [Semiconductors](#), said, "By the end of the project in 2010 we aim to have accelerated the chip development process in the extremely high frequency (EHF) range through use of new methods and simulation tools that will allow European chip developers to maintain a top position over the whole wireless communications spectrum."

The ICESTARS project is funded by the European Commission within its Seventh Research Framework Programme (FP7) and is led by NXP [Semiconductors](#). The German semiconductor company Qimonda will develop advanced analog simulation techniques, and MAGWEL of Belgium will focus on electromagnetic simulation. University partners include The Mathematical Institute of the University of Cologne (Germany), Upper Austria University of Applied Sciences, the University of Wuppertal (Germany), and the University of Oulu (Finland). The universities will concentrate on modeling, algorithmic problems, and simulation issues that must be solved to produce robust and accelerated automated testing of analog circuits with digital signal processing in the EHF region.



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