☒ **Public**

☐ **Confidential**

Project:	**ICESTARS**
Project Number:	FP7/2008/ICT/214911
Work Package:	WP2
Task:	T2.5
Deliverable:	D2.10 (v1.1)

Title:	Public report on the dimensioning tool for optimising the harmonic matching of an RF power amplifier
Author(s):	J. Aikio, M. Mäkitalo, T.Rahkonen
Affiliation(s):	University of Oulu, Finland
Contact:	timo@icestars.eu, janne@icestars.eu
Date:	30-Sept-2010

Table of Contents

1 Introduction

One of the major challenges in RF power amplifier (PA) design for modern wireless communication systems is to design Pas that are high linearity and decently ient. As PAs are rather nonlinear devices, also the mixing between harmonic bands is significant. Properly shaped harmonic bands (or harmonic injection) can be used for linearisation of a stand-alone amplifier. When external linearisation, e.g. pre-distortion is used, this mixing from harmonic bands is a major difficulty, however, as it causes bandwidth dependent distortion called memory effects, that is much more complicated to linearize than distortion components that do not depend on bandwidth. Especially distortion mixed from the envelope (DC) and 2nd harmonic band to the fundamental band has strong impact not only on the level of intermodulation distortion (IMD) but also on the asymmetry between upper and lower IMDs [1]-[3]. In fact, the optimization of harmonic impedances is the key for minimizing memory effects and distortion. Such approach has not been widely used due to the fact that the mechanisms of how harmonic tuning affects distortion cannot be monitored with the current distortion analysis tools. For instance, Harmonic balance (HB) simulation can only show the total distortion giving no details how the distortion is built up. Fortunately, several techniques based on Volterra analysis exists that are able to give more detailed insight of distortion and able to pinpoint the dominant causes of the distortion, cancelling mechanisms of distortion and even mixing gains between frequency bands i.e. pinpoint the memory effects [1]-[6].

In this deliverable a fast harmonic load pull analysis method is presented. The technique utilizes a recently within the ICESTARS project developed Volterra on top of HB (VoHB) [3],[6],[14] and a direct Volterra method (VoAC) [1],[2]. The concept of the analysis is such that first, one HB steady-state analysis is run to provide large-signal spectra of nonlinear VCCSs of the nonlinear device model. Based on these, the polynomial model for each nonlinear source (VCCS) is fitted on-the-fly with VoHB. Then the fitted polynomials are used in the direct Volterra method for distortion analysis in various harmonic impedance levels. The detailed distortion analysis for the found optimal impedances can be further analyzed with VoHB. With the proposed harmonic load pull method one can quickly minimize the level and asymmetry of IM3 but also flatten the IM3 response over a broad bandwidth.

2 Harmonic impedance optimization using Volterra analysis

The traditional load pull in which fundamental matching impedances are sought is widely used, while harmonic load pull is less popular. In fact, the practical impedance tuners for harmonic bands often can only cover a limited set of impedances. In the circuit simulator this is not the case, but the main limitations for the harmonic tuning are the convergence, accuracy and – especially - simulation speed. When combining HB with Volterra analysis we can achieve a fast, detailed and extensive analysis technique. One must note that in harmonic load pull we face a multi-dimensional optimization problem as we have to optimize at least four complex impedances ($Z_{IN}(f_{env})$, $Z_{IN}(f_{2H})$, $Z_{OUT}(f_{env})$ and $Z_{OUT}(f_{2H})$) simultaneously. If these impedances have bandwidth dependency, which often is the case, more variables are required. Therefore, harmonic load pull over the Smith chart becomes difficult to visualize and slow to set up, and a two-step procedure is used here: first, numerical optimization methods are used to find a good nominal position for each impedance, and then a full sweep over the entire Smith chart is performed for one impedance at a time, the others being held in their nominal positions.

The main idea in this analysis is that in a relatively linear RF PA the fundamental matching sets the large-signal operating point, while the effect of harmonic distortion is reasonably modest. Hence, one can use a Volterra model built in one operating point to perform an extremely fast sweep of the harmonic matching impedances, while keeping the fundamental matching fixed.

2.1 *Procedure of the Harmonic Load Pull Technique*

The procedure of the technique is as follows:

- First, the HB steady-state response of the circuit with some default terminal impedances (see Section 3.2) is simulated. The fundamental amplitudes are saved as well as large-signal spectra from each nonlinear VCCS.
- Second, the polynomial models for each nonlinear VCCS are fitted based on the simulated large signal spectra.
- Third, envelope and second harmonic input and output impedances are optimized or systematically swept. The simulated fundamental amplitudes and fitted coefficients are used for direct Volterra method (VoAC) to calculate $IM3_L$ and $IM3_H$ (upper and lower IM3) response at each set of impedances.
- Fourth, the IM3 response in the optimized impedance point is analysed using VoHB, accuracy comparison between Volterra and HB is performed and IM3 contour plots near the optimized impedances are shown.

In order to illustrate the procedure the flowchart of the harmonic load pull technique is presented in Fig. 1.

The idea of this approach is that VoHB is simulated after HB to update the coefficients and then fast direct Volterra calculations with fixed models are used within an impedance optimization loop or harmonic load pull, where the large number of analyses needs to be calculated. Finally, distortion contribution analysis using VoHB can be performed in order to see the reason for the linearity improvement and verify its robustness.

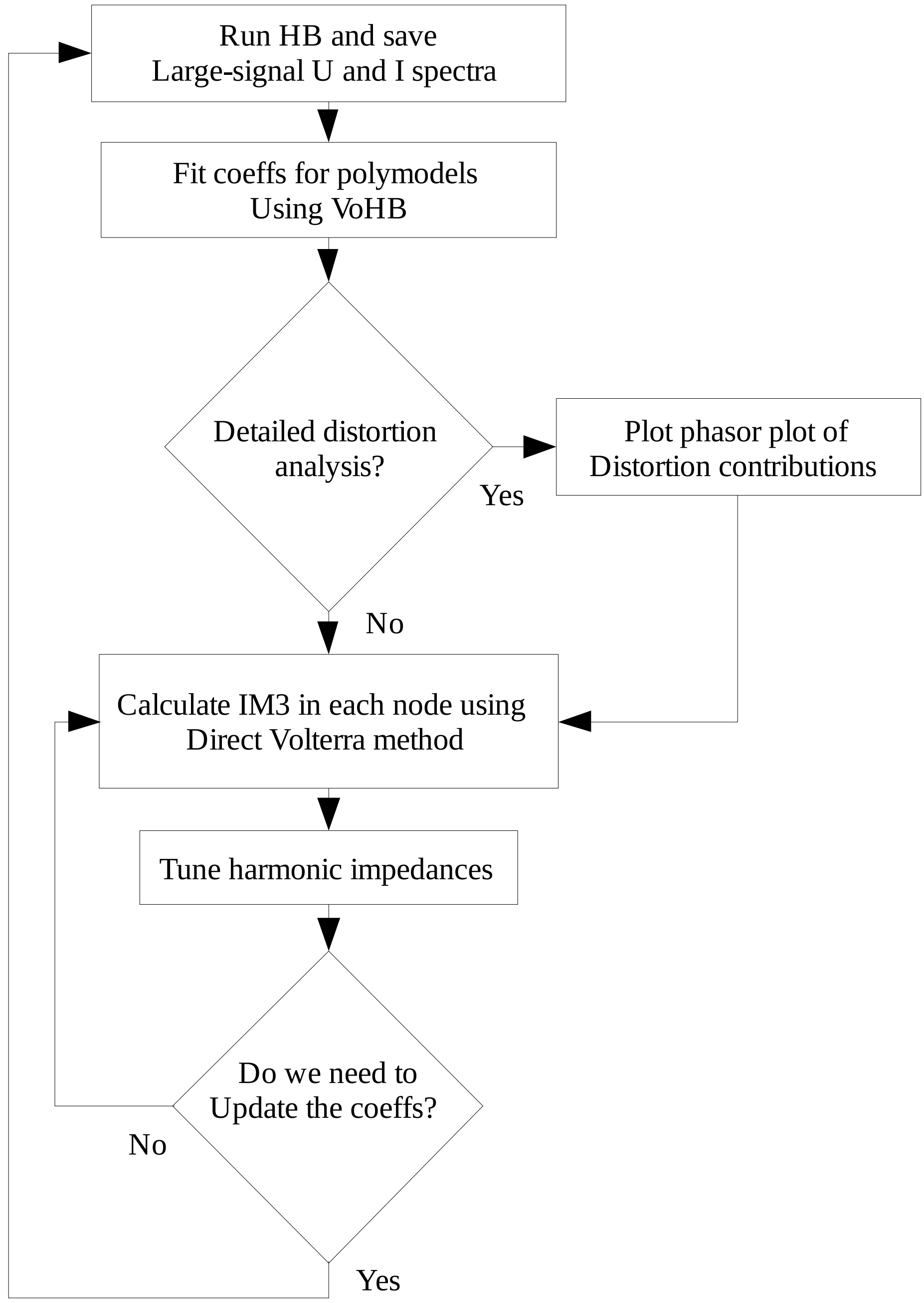

Fig. 1 Flowchart of the harmonic load pull technique. The loop is exited when IM3 meets the specs or number of iterations is exceeded.

2.2 *Accuracy Considerations*

The Volterra analysis is obviously prone to errors due to the fact that the polynomial coefficients may chance during the impedance optimization. The fact that fundamental impedances are fixed (i.e. operation conditions of the device remain rather constant) actually allows Volterra analysis to be successfully used. However, when impedances are far from the fitted values large errors might occur. Therefore, here optimization has been implemented in five phases. Between each phase calculated results between Volterra and HB are compared and coefficients are updated. In this way we can assure that the achieved linearity improvements are accurate. Thus far coefficients are not updated during systematic impedance sweep, but as the results in Fig. 6 show (see Section 4.1.2) the largest error often occurs at the point of highest distortion, which is usually far from the optimum point. In the desired distortion minimum the match between HB and VoAC is good.

3 Implementations

The prototype for harmonic impedance optimization was set up in the APLAC circuit simulator [7], in which the VoHB technique and direct Volterra method up to 3rd degree were implemented first using APLAC's command language (I-language) and then in C using APLAC's AIF interface [3]. The testing reported here was performed using APLAC's command language version.

3.1 *Volterra Implementations*

Calculation of $IM3_L$ and $IM3_H$ is implemented in the Volterra calculation, which allows the IMD asymmetry to be detected and minimized. The direct Volterra method contains three calculation steps: First, 2nd-degree distortion currents of all nonlinear sources at f_H-f_L are calculated. The voltage response of these currents is then calculated in each node with the use of the transfer functions of the circuit. The voltage response at frequency f_L-f_H is a complex conjugate of $v_n(f_H\text{-}f_L)$. Then, the 2nd-degree distortion voltages at the $2\cdot f_L$ and $2\cdot f_H$ are calculated in a similar manner. And finally, previously calculated 2nd-degree distortion voltages are used to calculate the $IM3_L$ and $IM3_H$ voltage response in each node. The flowchart of the implemented Direct Volterra is shown in Fig. 2.

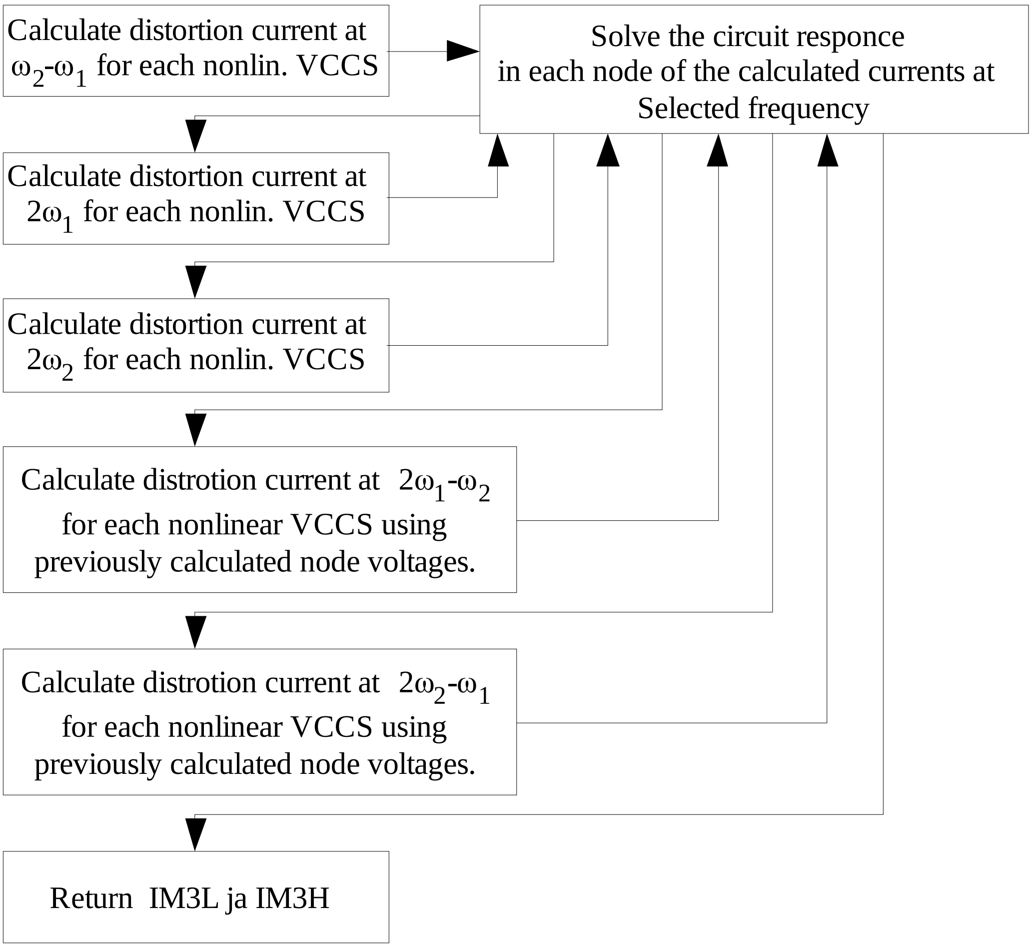

Fig. 2. Flowchart of the Direct Volterra calculation.

3.2 *Circuit test setup*

For testing purposes a test bench based on the LDMOS PA was constructed in APLAC. The used transistor model is Freescale's intrinsic LDMOS MET model [8] MRF21030 [9], which contains narrowband internal matching. However, for testing purposes it is more convenient to optimize the input and output impedances as directly seen by the wideband intrinsic transistor than via heavy matching circuitry. In this way we can see the direct impact of the varied impedance and thus test the analysis power of the technique. Therefore the internal matching was removed from the model and replaced by table-based generic impedance (Zblock).

The simulation test setup is presented in Fig. 3. The test circuit contains three nonlinear Q-V sources C_{GS}, C_{GD}, C_{DS} and one nonlinear I-V source I_{DS} that is controlled by both input and output voltages V_{GS} and V_{DS}. 1-dimensional 3rd-degree polynomial model was fitted for Q-V sources and 2-dimensional 3rd-degree model for I_{DS}.

The default impedance values for the test bench were obtained by simulating the matching circuitry of the complete MRF21030 LDMOS PA [9]. Obtained input and output impedances seen by the intrinsic transistor at each frequency of a 3rd-order analysis were written in the Zblock elements (Z_{IN} and Z_{OUT} in Fig. 3) that are simply tables of impedances. In Zblocks the fundamental impedances were fixed for optimum gain and power match, respectively. The 3rd harmonic impedances were set to zero whereas the envelope and 2nd harmonic impedances were allowed to be optimized. Due to the fact that the envelope and second harmonic impedances are bandwidth dependent this was taken into account as well. Thus, at the second harmonic impedances $Z(2\cdot f_L)$ and $Z(2\cdot f_H)$ were allowed to vary independently while $Z(f_L+f_H)$ located between $Z(2\cdot f_L)$ and $Z(2\cdot f_H)$ is calculated as a mean of $Z(2\cdot f_L)$ and $Z(2\cdot f_H)$. Envelope impedances have initial values typical to normal biasing circuits.

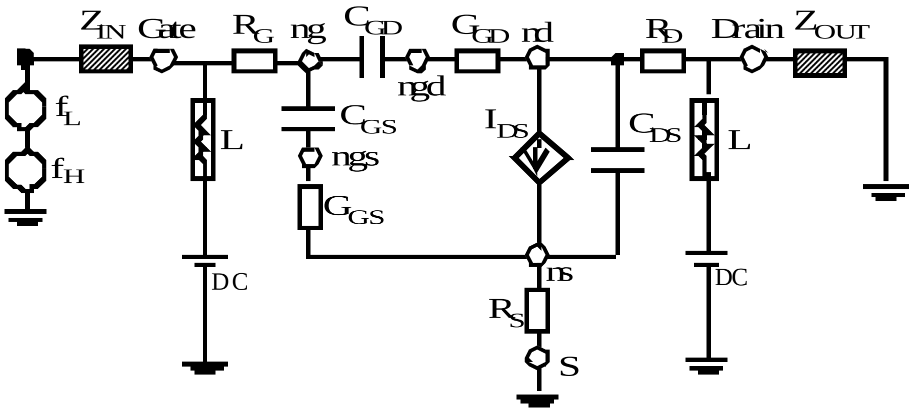

Fig. 3. Test setup for harmonic impedance optimization

The centre frequency for the 2-tone test signal was 2.14 GHz. The amplifier was biased in class AB (I_{DQ}= 450 mA). The input amplitude was set to 5 dBm/tone and the tone spacing f_H-f_L was set to 300 kHz.

4 Simulations

Provided that the load pull sweep is fast enough, the optimum impedances could be searched manually by moving markers on a Smith chart, for example. The current implementation is very close to that as Volterra analysis impedance sweep of a single-transistor PA over 6400 different impedance points takes only 4 seconds. However, due to multitude of simultaneous variables, it is still faster to find a good nominal value for all impedances by numerical optimization instead of manual tuning, and then study the sensitivy by a full load pull sweep. Both Multi directional search optimization (MDSearch) [10] and MinMax optimization method [11] with different amount of iterations were tested, and an initial search by MDSearch, followed by a longer (but fast) MinMax optimization with gradually tightening goals seemed to be a well-functioning solution for finging a good nominal operating point.

4.1 *Simulation example*

The single-transistor PA in Fig.3 was optimized so that after the initial HB and model fitting, a good nominal point for the harmonic impedances was first optimized using the combined MDSearch and MinMax. Weighting of the goal function was gradually changed during the optimization, and a total of 300 MDSearch+4x100 MinMax iterations were run using Volterra analysis. Addition to this, 6 HB and VoHB runs for re-fitting were done, and all these together takes only 27 and 0.93 seconds with the I and C language implementations, respectively. This minimizes the level of $IM3_L$ and $IM3_H$ as well as IMD asymmetry.

After this we can perform a systematic impedance sweep (harmonic load pull) near the optimized impedances to see the sensitivity of the optimum. This results in four contour plots of $Z_{IN}(f_{env})$, $Z_{IN}(f_{2H})$, $Z_{OUT}(f_{env})$ and $Z_{OUT}(f_{2H})$ in the Smith chart that can be used for visual inspection of the broadness of the minima. If a flat IMD response with minimum IMD asymmetry over a broad bandwidth is required then an additional Min-Max optimization can be performed while sweeping the tone spacing of the 2-tone test signal. The flowchart of the simulation procedure is shown in Fig. 4.

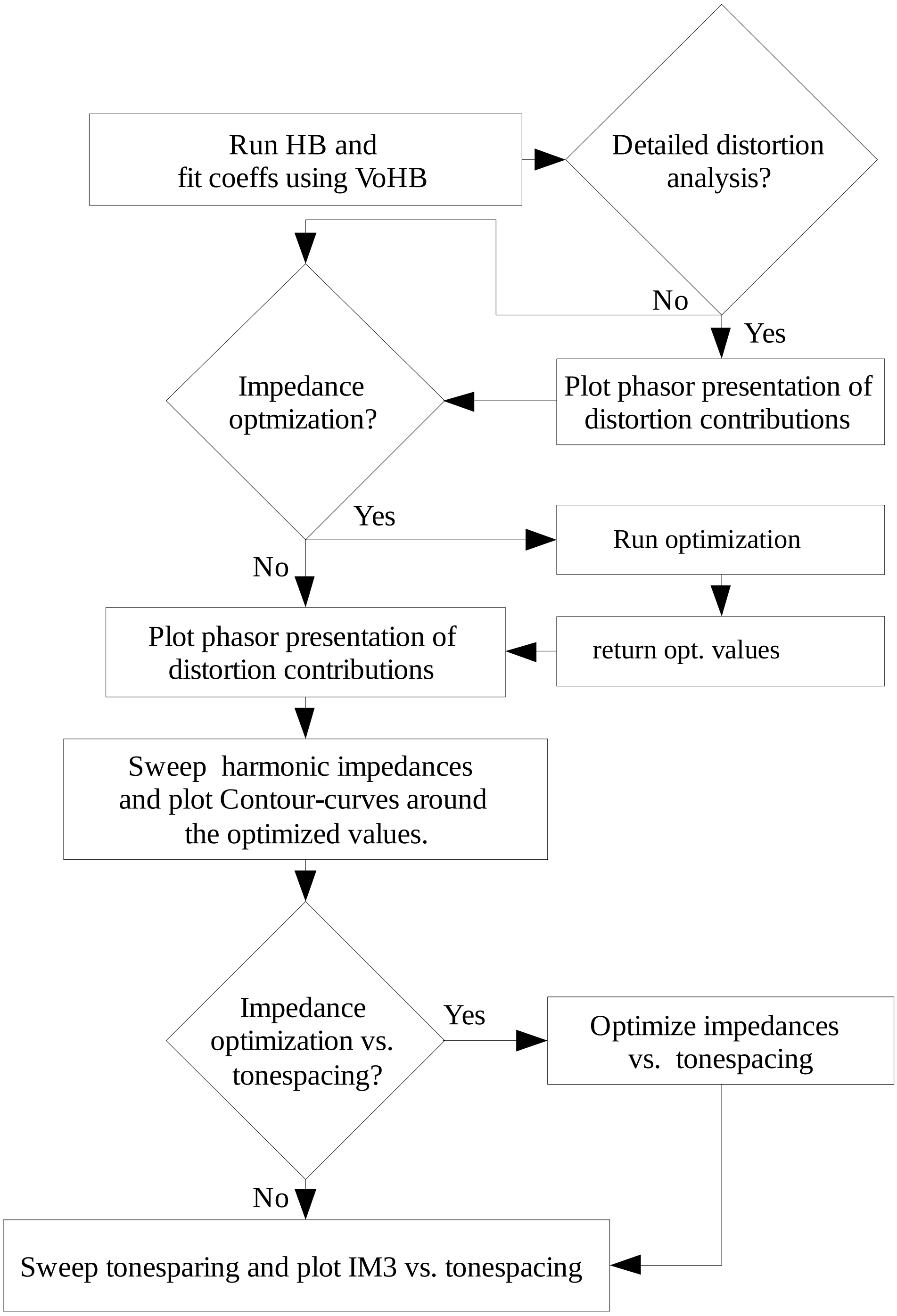

Fig. 4. Flowchart of the simulation procedure of harmonic load pull.

4.1.1 Phasor Presentation of the Optimization

The phasor plot of the contributions of the total $IM3_L$ at the drain node and more detailed view of the dominating I_{DS}-V_{GS}-V_{DS} source with default impedance values are presented in Fig. 5 a) and b). From Fig. 5 a) it can be seen that the $V(I_{DS})$ dominates the IM3 while the effect of the capacitances is rather small. The detailed view of the $V(I_{DS})$ presented in Fig. 5 b) shows that the cubic nonlinearity $V(K_{30}\cdot V_{30})$ is the dominant distortion contribution. The 2nd-degree distortion mixed to IM3 from the 2nd harmonic band $(V(K_{20}\cdot V_{H2}))$ is in the same phase and thus increases the nonlinearity of the source. Negligible contributions are not shown in the phasor plots.

After 700 optimization cycles of the harmonic terminations both $IM3_L$ and $IM3_H$ have decreased from -32 dBm (-45 dBc) to -55 dBm (-68 dBc). The level of the fundamental tones is practically unchanged. The phasor presentation of the optimization can be seen from Fig 5 c) and d). Now $V(I_{DS})$ no longer dominates the IM3 as it is small compared to the nonlinearity caused by the nonlinear capacitors. The more detailed view of the $V(I_{DS})$ presented in Fig. 5 d) shows that after the optimization the cubic nonlinearity remains the same but now the 2nd-degree distortion mixed from the envelope band $(V(K_{20}\cdot V_{ENV}))$ is in the opposite phase and thus cancels the cubic nonlinearity almost completely. Note also that $V(K_{20}\cdot V_{H2})$ has become rather small. Hence, it can be concluded that the impedances of the second harmonic have been minimized and that the envelope impedances have been optimized to cancel the large cubic nonlinearity.

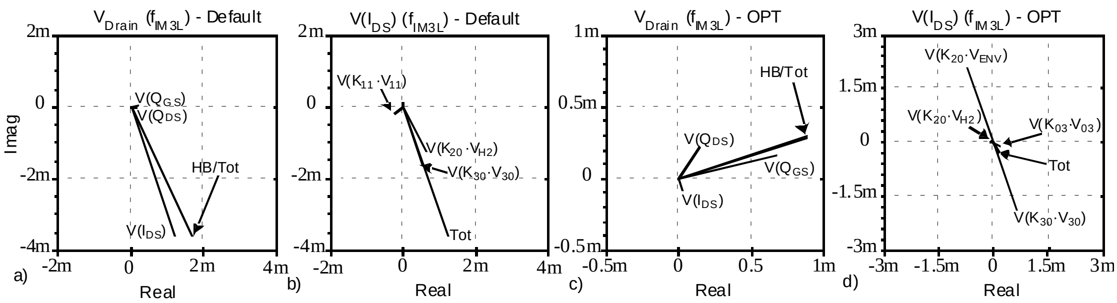

Fig. 5. Phasor presentation of the a) total IM3L at the drain node and b) contributions of I_{DS}-V_{DS}-V_{GS} source before the optimization and phasor presentation of the optimized c) total IM3L at the drain node and d) contributions of I_{DS}-V_{DS}-V_{GS} source.

4.1.2 Contour Plot of the Simulations

In order to monitor broadness of the found optimum a systematic impedance sweep around the optimum point is run and the contour plots of the impedances are drawn to the Smith chart. This is an visual way also to see if the impedances are realizable. As an example, a 80·80 grid in the squared area around the previously optimized $Z_{OUT}(f_{env})$ was simulated and the results are shown in Fig 6 a). The optimized value very close to point (-1,0) is marked with a cross (-55 dBm) surrounded by the -50 dBm...-15 dBm contour curves. From the figure it can be seen that very little variation in $Z_{OUT}(f_{env})$ is allowed in order to maintain the achieved linearity. In fact, the strong cancellation is always sensitive to the impedance variations and thus achieved linearity will be difficult to maintain in practice.

An important question is whether the Volterra model fitted in one operating point remains valid over the entire sweep. This has been verified by comparing the results of Volterra calculation and HB analysis in each grid point. The error contours of the worst case are shown in Fig. 6 b). It can be seen that the error grows to several dB's, but only in the area where also the distortion peaks due to coherence of the distortion contributions. Close to the optimum point the error remains within one dB, which justifies the use of the Volterra analysis.

When comparing simulation time between HB and Volterra, 4·80·80 load pull points were calculated meaning almost 26000 analysis. For HB this means 13 minutes. The Volterra calculation in I –language version takes 2.5 minutes, but only 6 seconds in C-language version. Hence, the entire optimization and analysis are performed in almost real-time.

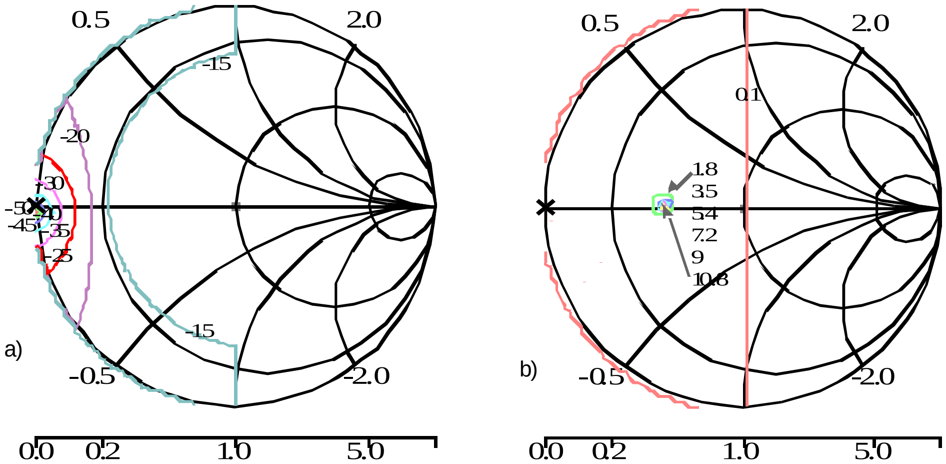

Fig. 6. Contour plot of a) IM3L with varying $Z_{OUT}(f_{env})$ and b) error contour plot of $Z_{OUT}(f_{env})$ between Volterra and HB (in dBs).

4.2 *Optimization of the Broadband Response*

When optimizing the IMD also with respect to bandwidth we face somewhat more complex optimization problem. This feature still needs some development, and the results are demonstrated by a circuit, where the MET model is replaced with VCCS models with fixed polynomial coefficients.

The optimized impedance values with fixed tone spacing often result in poor IMD improvement when tone spacing is varied. This is inherently true as can be seen from the upper curves in Fig. 7 a), where the IM3 response vs. tone spacing is presented. The IM3 response is good at the optimized tone spacing f_H-f_L=300 kHz but then worsens dramatically. The response shows also IMD asymmetry couple of dBs. The bandwidth dependency of IM3 was optimized using 100 cycles of minmax within 40 different tone spacings between 0 and 20 MHz. The optimized results (lower curves in Fig. 7 a)) show almost flat IM3 response with very small IMD asymmetry. The optimized values of the $Z_{IN}(f_{env})$ and $Z_{OUT}(f_{env})$ at different tone spacing are presented in Fig. 7 b) and c). No guarantees are given whether these impedances are realizable but they offer excellent starting point for the designer.

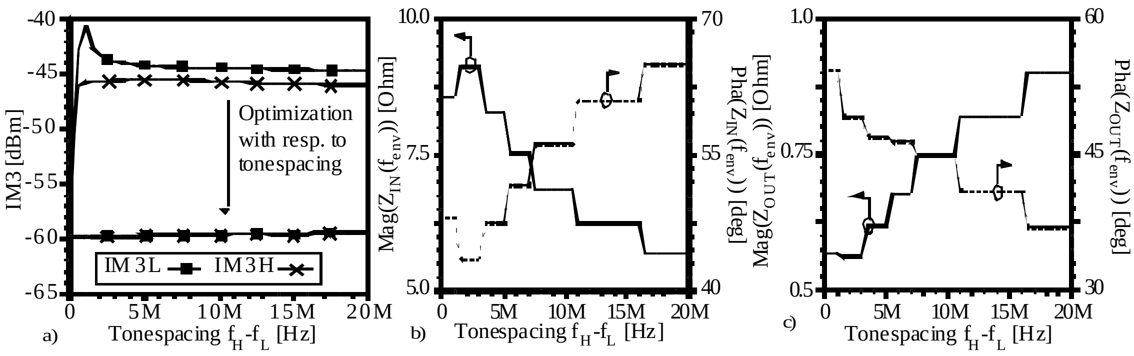

Fig. 7. a) IM3 tone spacing before and after tone spacing optimization and the optimized b) Z_{IN} and c) Z_{OUT} values at the envelope band.

5 Summary

In this deliverable we have presented the harmonic load pull technique based on the Volterra analysis. The idea was first tested with a command language prototype (limited to single-device amplifiers only) reported in [13] and then re-coded in C language. Some simulation results are reported in [13].

The analysis proceeds as follows: After an initial HB simulation the polynomial models for each nonlinear source are fitted and these are then used for direct 3rd-order Volterra calculation. This allows very fast nonlinear analysis and also detailed distortion analysis is possible to show the causes and robustness of the obtained linearity improvement. The technique is implemented in APLAC and shows significant analysis speed improvement compared to HB: a full 4-variable load pull sweep that takes 13 min using HB is completed in 2.5 min using i-language Volterra analysis, and in less than 6 sec with c-language implementation. This is fast enough also for manual fine-tuning. As harmonic load pull does not change the signal waveforms very dramatically, the once fit Volterra model gives sufficient accuracy especially around the optimum point.

The next obvious step is to characterise typical biasing and matching circuits so that a proper structure can be chosen based on the relative positions of the envelope, fundamental and 2nd harmonic impedances found by the Volterra load pull. This part was left outside of the project.

6 References

[1] P. Wambacq, W. M. C. Sansen, *Distortion Analysis of Analog Integrated Circuits*. Kluwer Academic Publisher, 1998.
[2] J. Vuolevi, T. Rahkonen, *Distortion in Power amplifiers.* Artech House, 2003
[3] Janne P. Aikio Frequency domain model fitting and Volterra analysis implemented on tops of harmonic balance simulation. PhD dissertation in University of Oulu, Oulu, Finland. Available at http://herkules.oulu.fi/isbn9789514284205/
[4] A. Heiskanen, J. Aikio, T. Rahkonen, "A 5th-Order Study of a 30W LDMOS Power Amplifier." In *Proc. IEEE Int. Symp. Circuits and Systems*, Vol. 4, 25-28 May 2003.
[5] L. Peng, L. T. Pileggi, "Efficient Per-Nonlinearity Distortion Analysis for Analog and RF Circuit." *IEEE Trans. Computer Aided Design*, Vol. 22, No. 10, pp. 1297-1309, October 2003.
[6] J. P. Aikio, T. Rahkonen, "Detailed distortion analysis technique based on large-signal voltage and current spectra." *IEEE Trans. Microw. Theory Tech.*, vol 53, no. 10, pp. 3057-3066, Oct. 2005.
[7] APLAC circuit simulator, Espoo, Finland. [Online]. Available: http://www.aplac.com
[8] W. R. Curtice, J. A. Pla, D. Bridges, T. Liang, E. E. Shumate, "A new dynamic electro-thermal nonlinear model for silicon RF LDMOS FET's." *1999 IEEE MTT-S Int. Microwave Symp. Dig*, vol. 2, pp. 419-422.
[9] Freescale, Austin TX, MRF21030 LDMOS power transistor data sheet, [Online]. Available: http://www.freescale.com/files/rf_if/ doc/data_sheet/MRF21030.pdf
[10] J. E. Dennis, Jr., and V. Torczon, "Direct Search Methods on Parallel Machines," *SIAM Journal of Optimization*, vol. 1, no. 4, pp. 448–474, 1991.
[11] S. Maas, *Nonlinear Microwave Circuits*. Norwood, Massachusetts: Artech House, Norwood, Massachusetts, 1988.
[12] J.P.Aikio, M. Mäkitalo, T. Rahkonen, "Harmonic Load-pull Teachnique based on Volterra Analysis" Proceedings of the 39th European Microwave Conference, pp. 1696-1699, Rome, Italy, Sept. 2009.
[13] Mäkitalo, M. "Optimization of RF-amplifier's distortion using harmonic impedances" University of Oulu, Department of Electrical and Information Engineering, 2009. Master's Thesis (In Finnish).
[14] T. Rahkonen, J. Aikio: "Public report on the electro-thermal fitting and Volterra analysis". Deliverable D2.9 of the same project (FP7/2008/ICT/214911