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1. Abstract 3
2. Introduction 4
3. Impact of the ICESTARS results on European industry 6
3.1 Semiconductor market and EDA tools 6
3.2 ICESTARS partners in European contents 6
3.3 Socio-economic and scientific impact of ICESTARS 7
4. Dissemination 9
4.1 Dissemination methods and media 9
4.1.1 Public ICESTARS project webpage 9
4.1.2 ICESTARS internal wiki 9
4.1.3 Email reflector lists 10
4.1.4 Press releases 10
4.1.5 Conferences, workshops and scientific papers 11
4.2 Dissemination plan of academic partners 13
4.2.1 Universität zu Köln 13
4.2.2 Bergische Universität Wuppertal 13
4.2.3 Fachhochschule Oberösterreich 13
4.2.4 University of Oulu 13
4.2.5 Helsinki University of Technology 13
4.3 Dissemination plan of industrial partners 13
4.3.1 NXP 14
4.3.2 Infineon 15
4.3.3 AWR APLAC 15
4.3.4 MAGWEL 15
5. Exploitation 16
5.1 Use plan of industrial partners 16
5.1.1 NXP 16
5.1.2 Infineon Technologies 17
5.1.3 AWR APLAC 18
5.1.4 MAGWEL 18
5.2 Use plan of academic partners 20
5.2.1 Universität zu Köln 20
5.2.2 Bergische Universität Wuppertal 20
5.2.3 Fachhochschule Oberösterreich 20
5.2.4 University of Oulu 20
5.2.5 Helsinki University of Technology 21
6. Intellectual Property 22

1. Abstract

This document outlines the initial Dissemination and Use Plan, detailing the envisaged exploitation of ICESTARS project results. The diverse background of the ICESTARS partners (4 academic and 4 commercial partners) guarantees the balance between the dissemination of the project results, i.e., making them available outside the limited group of project partners, and the commercial usage of gained knowledge in day-to-day design activities to improve the competitiveness of the European semiconductor companies and EDA tool providers. The Dissemination and Use plan highlights the economic, scientific and social impact and the benefits of the project for different target groups. In alignment with their professional objectives and standard activities the academic partners will focus more on the dissemination of the results, while industrial partners will concentrate more on the fast inclusion of the results in their design tools and products. The dissemination efforts will be coordinated by partner KLN, while the exploitation of the results will be coordinated by partner INF.

2. Introduction

The Dissemination and Use Plan is the basis of Knowledge Management within the ICESTARS. It contains plans to disseminate project results, both within the ICESTARS Consortium and externally, as well as the envisaged use of the project results beyond the project duration. In this document we describe both general strategies of the Consortium as well as the individual dissemination and usage approaches of academic and commercial partners. Since dissemination is an important and rather natural task for academic institutions, whereas exploitation is ranked more important in an industrial environment, it has been decided to entrust KLN with coordination of dissemination and INF with coordination of exploitation of results coming out of ICESTARS.

The Dissemination and Use Plan includes the management of knowledge going into the project, created within the project, and going out of the project, including Intellectual Property Rights (IPR) protection. The following table gives an overview of the Knowledge Management Plan.

Knowledge	What	Expertise / Responsible	Plan
Into ICESTARS	Investigation of State-of-the-Art	Advisory board, Project Officers, Review auditors	Timely knowledge of the State-of-the-Art, keeping informed on progress in the field
within ICESTARS	Exchange of knowledge	Coordinator, WP 4	Web based communication structure
	Creation and protection of knowledge	Coordinator, WP 4 – Task Intellectual Property	See Section 6
out of ICESTARS	Dissemination	All, WP 4 – Task Dissemination	See Section 4
	Exploitation	All, WP 4 – Task Exploitation	See Section 5

Table 2-1 – Knowledge Management Plan

While the Dissemination plan focuses on strategies for distribution of information about the project progress and achieved results, the Use plan gives an outlook on the partners' intentions with respect of the exploitation of the project results to add commercial and scientific value to their respective companies and institutions.

The Dissemination plan of the ICESTARS project involved activities in

- Dissemination of the project results among partners and end users
- Interaction with the research community
  - Publications in leading journal papers
  - Participation in related scientific conferences
  - Organisation of the ICESTARS Workshop

The Use plan of the ICESTARS will cover the following aspects

- Educating target users about the novel wavelet-based techniques for circuit simulation and driving the new technique into productive use
- Exploitation of developed envelope/multirate algorithms to speed up simulation of RF circuits
- Improvement of the existing RF simulation tools based on Harmonic Balance engine to maintain the leading position of the European semiconductor companies

- Educating target users about the promising Volterra on Harmonic Balance approach to enable accurate design of highly non-linear power amplifiers and driving the generated code into a productive/commercial use
- Exploitation of developed coupled ElectroMagnetic-Circuit analysis approaches to further the mixed-signal designs by characterizing and optimizing the functional devices taking into account the electromagnetic interaction between neighbouring devices.
- Enhancing the state-of-the-art in science and education by
    - Incorporating the gained knowledge in university courses
    - Exploiting the new results as a basis for further research and support of young researchers pursuing their MSc. and PhD. theses

All partners are actively involved in the dissemination of knowledge and the publications in the appropriate scientific journals, contributions to conferences, etc. are stimulated and supported within the Consortium. These activities are important both to demonstrate and benchmark the scientific advances of ICESTARS partners to the global scientific community. The authors of technical/scientific publications are responsible for the contents of their contributions. They are obliged to notify the project coordinator of all dissemination activities and the coordinator will make sure that IPR and other issues are taken into account. In particular, all project related publications need approval of all partners. The project manager is responsible for dissemination of the results of the project as a whole. The outcome of the dissemination activities is reported in the mid-term meetings as well as the annual Project Review meetings.

Finally, wherever the opportunities for standardisation or patent applications arise, the individual partners will certainly do this. Property rights occurring from work done in ICESTARS will be dealt as prescribed in the Consortium Agreement and the general conditions of the EC.

3. Impact of the ICESTARS results on European industry

3.1 Semiconductor market and EDA tools

The ICESTARS project is a combined effort of the leading European semiconductor companies and design tool providers together with European universities to harness the power and promise of nano-technologies towards a networked society. As such, the project has a strong strategic impact according to the visionary goals of the IST programme. Quoting from a Gartner Research Note (SPA-18-8621, Dec. 2002):

- By 2008, more than 30 percent of Internet access in the home will be through non-PC wireless devices (0.6 probability).
- By 2012, radio frequency identification (RFID) and similar wireless chips will evolve from a supply-chain technology into an enabler of value-added consumer applications, such as item location and status reporting (0.6 probability).

The above predictions, together with the general vision of embedded connectivity and ambient intelligence (where computers and networks will be integrated into everyday life) could well become a reality due to the promise of nano-technologies and the general advance in process and fabrication technologies. In the high-tech sector, Telecommunications and Microelectronics are key enablers of jobs and economic growth in the European Union. The development of microelectronics is at the very heart of future economic developments in products and services of the ICT sector. There is no area of modern life untouched by the progress of microelectronics. Thanks to advances in microelectronics new market opportunities are emerging in Europe characterized by the needs of products and services offering both mobility and connectivity. Europe has a solid industrial base, especially in Telecommunications, Home Electronics and Car Electronics (automotive) and is well profiled for this future growth.

However, the large investment in nanoelectronics process technology and the development of advanced transistor and interconnect technologies is obsolete without accompanying design tools commonly referred to as Electronic Design Automation (EDA) tools. The industry acceleration towards smaller technology nodes (currently at 65nm, shrinking down to 4x/3x nm and further to 18nm nodes) and the ever-increasing complexity (i.e., transistor count in terms of tens of millions per chip) of integrated circuits makes EDA tools obligatory in the manufacturing process. Furthermore, the importance of shortening the time to market and stronger industry focus on reliability and yield necessitates the robust, fast and accurate design tools based on top-class numerical algorithms.

Although there has been a long tradition that the design tools are provided by US-based companies, new opportunities arise at every technology generation. Start-up companies (SMEs) address design concerns that are difficult to address by established software providers because the overall tool sets are too rigid to deal with the fast change of design demands. This explains why the traditional software vendors acquire the modern tools by purchase more than by in-house development. Their role shifts from software development to software integration. As such, those companies forego part of their role as technology leaders and lose partial control over the pace of tool development and innovation. However, the product and services-oriented European companies still critically depend on those environments for next-generation product design and development that can keep them updated with the rate of innovation in their own fields. As such they require that development in tools and methodologies keeps pace with the technological progress and be readily available for immediate productive use.

3.2 ICESTARS partners in European contents

The ICESTARS project is a key project to impact the position of Europe's semiconductor industry in critical and strategic semiconductor market sector. More importantly, without the ICESTARS project

there would be a delay in bringing more effective IC design to European semiconductor industry, which would severely impact Europe's current strength in this important hi-tech area. Many companies throughout Europe would find it difficult to compete on a world stage without state-of-the-art IC design tools.

The European semiconductor industry, together with leading research institutes and academia, have proven their capability to co-operate successfully in European wide programs like JESSI, ESPRIT, MEDEA, MEDEA+ and IST. These programs have helped the European semiconductor companies to catch up in technology, which has led to the indispensable improvement of the performance of that industry. The ICESTARS consortium is the latest effort in this respect, having immersed from another strong co-operative European initiative: FENICS, the First European Network for Industrial Circuit Simulation. This network was founded in 2004 by Europe's major semiconductor industries (NXP, Qimonda/Infineon, Nokia and ST) in order to coordinate research efforts, and has been very active since with quarterly meetings.

A European approach to achieving the project's objective has a number of advantages. While acknowledging that a great deal of expertise is available at the national level amongst scientists and engineers, this expertise is unevenly dispersed between countries. Both in the Netherlands and in Germany, the respective semiconductor companies of the ICESTARS consortium have built up a large network of academic partners, but they have concentrated on different issues. Infineon/Qimonda has mainly fostered work in national projects on advanced methods for transient simulations, while NXP created a local environment concentrating on the development of computational electromagnetics simulations and dynamic partitioning. A similar observation holds for the SMEs: AWR-APLAC has built-up expertise on frequency domain simulations due to a strong Finnish network of academic institutions working in this area and their strong connections to Nokia, whereas MAGWEL benefits greatly from the knowledge available in the Leuven area on semiconductor device design and simulation.

ICESTARS consortium operating on a European level therefore provides benefits in terms of introducing new technologies and experience from different countries, combining technologies in complementary fashion, disseminating the technologies to end-users at a European scale, and proposing a code of standards Europe-wide. Dissemination of the ICESTARS results outside the participating partners will be established by "open" workshops, publications in leading journals, conference presentations, and via the ICESTARS Website

3.3 Socio-economic and scientific impact of ICESTARS

Being essential for the design of future RFICs, e.g. for high data-rate wireless applications, the socio-economic impact of the ICESTARS project can be traced via its contribution to the creation of a communication infrastructure that allows the user to communicate anything, anytime, anywhere, to anybody, in an affordable, interactive and intuitive way. Such an infrastructure enables a large number of uses that will revolutionize society in all its facets. This will include applications like *e* - commerce, *e* - business, *e* - work, *e* - learning, *e* - health, *e* - safety, *e* - governance and many more.

The *economic impact* of the creation of such an infrastructure is large. It entails the creation of new markets (for hardware / software / content / services) and more efficient business processes (leading to higher productivity / agility). In turn, the new markets lead to the creation of new, high-quality, jobs (both direct and indirect), whereas the more efficient business processes will improve the competitive position of companies in the market.

The *scientific impact* will be large as well. First and foremost, this holds for advances over the state-of-the-art in the field of nanoelectronics. Second, results obtained are not restricted to the problem areas considered in this FP7 call, but also to other areas of application. Systems of DAEs having a similar structure arise in many other fields such as in mechanics (e.g. multibody problems, crash tests, mechanical oscillations), in fluid dynamics and material science. It is expected that, based on the novel PDAE approach, the techniques to be developed in this project will have a significant impact on the progress of numerical simulation methods in the above mentioned research areas.

Last, but not least, the *social impact* is equally high. During the last 20 years microelectronics influenced quality of life and health and safety more drastically than any other introduction of a new industry, due to increased switching frequency of the devices, miniaturisation and better and faster designs. This will cause even more changes in our future society due to mobility and communication, changing the lives of the European citizens drastically, boosting applications of which only a few are mentioned:

- **Learning:** The vision of conducting a fully interactive class session, including showing of items, such as maps, articles or experiments.
- **Working:** The key to this new trend of working from home will be aided by ICESTARS. This will allow people working at home to feel like they are working in the office.
- **Healthcare:** Getting better, faster and more accurate diagnosis will be possible if communication between the patient's home and the medical centre is improved (remote monitoring).
- **Aids for disabled people:** For those who have only the choice between either working from home or not being able to work at all, evolved modern communication techniques are extremely important.

Most of the above mentioned applications require broadband access to the infrastructure, which when added together, leads to an enormous capacity demand on that infrastructure. This demand can only be satisfied if the infrastructure operates at (very) high data rates. In turn, this requires hardware capable of operating at very high frequencies. Coupled with the demand for low-cost, small-size and low-power consumption, this leads to a major role for microelectronics. With the development of an essential enabler in this area, the ICESTARS project takes a fair share in the (large) socio-economic impact of the intended communication infrastructure.

4. Dissemination

It is of fundamental importance to the consortium that the knowledge generated in the proposed project is shared with other research groups and companies in order to:

- Generate broader acceptance for the developed technology and its applications
- Inspire more research projects in the area
- Generate interaction and feedback from other groups and learn from their experience
- Generate other positive benefits to the consortium or the European Community

Therefore, the dissemination programme includes:

- Organisation of seminars and workshops.
- Participation in important conferences and workshops, such as SCEE, DATE, DAC, ECMI, ECCTD, SPI, PIERS, etc.
- Publication in top-level scientific journals
- Information will also be published in the popular press.
- Public information about the project results via the public project web page http://www.icestars.eu
- Internal information exchange via the internal project web page http://wiki.icestars.eu
- Publication of the results in the various web sites of the European Commission, especially CORDIS PROJECTS and CORDIS RESULTS.
- Demonstration of the results to visitors from companies and research institutions all over the world.
- Use of ICESTARS results in the educational process, for training of students in the universities of the consortium.

The experience of the academic partners is essential for analysing and developing new methods for the modelling of complete RFIC blocks. In addition, by virtue of their direct educational involvement, they are in a prime position to translate the knowledge resulting from the ICESTARS project directly into the educational system. This direct link should not be viewed lightly as it constitutes a very relevant added value for European universities and European students. The availability of first-hand knowledge of the state-of-the-art in such brain-intensive technological areas is a key to maintaining Europe's expectations and presence and to the development of leading technical expertise in Europe.

4.1 Dissemination methods and media

4.1.1 Public ICESTARS project webpage

The public webpage http://www.icestars.eu is intended to inform about the research activities and results of the ICESTARS project. It will contain download areas for ICESTARS publications, deliverables, workshops and conferences.

4.1.2 ICESTARS internal wiki

The ICESTARS wiki http://wiki.icestars.eu serves as a convenient platform for the internal information exchange for the project members. Each project partner has access to the wiki and uses it for the administration and documentation of all management and research activities of the project. A project calendar informs about the upcoming events. All meetings (including phone meetings) are reported. It includes invitation letters, agendas and minutes.

Each work package has its own documentation area for exchanging activity plans, working documents, data files, deliverables and publications. It allows each partner to see the status of progress of all work packages with respect to all aspects of the project at any time.
Additionally the wiki is used to share templates and administrative documents as well as to keep contact data up to date.

4.1.3 Email reflector lists

Email reflector lists have been established for comfortable communications. They allow easy contact to all ICESTARS members at once but also to various groups as project management members or members of a certain work package.

4.1.4 Press releases

One press release has been published on November 4, 2008. The information has been spread all over the world in various languages. The following links show a few samples of more than 100 press releases informing about the ICESTARS project.

- Schnellere drahtlose Datenübertragung on infoweek.ch website (05/11/2008).
- Breaking Barriers For Next Generation Wireless Chips on sciencedaily.com website (04/11/2008).
- New Mathematical Algorithms to Break Barriers for Next Generation Wireless Chips on azom.com website (04/11/2008).
- Das Mathematische Institut der Universität zu Köln forscht im europäischen Projekt ICESTARS on the ExtremNews website (04/11/2008).
- ICESTARS: Drahtlose Kommunikationschips der nächsten Generation on the website of Kölner Wissenschaftsportal (04/11/2008).
- Innovativer Chip on rundschau.co.at website (04/11/2008).
- Drahtlose Datenübertragung wird beschleunigt on Innovations Report website (05/11/2008).
- AWR joins European wireless design effort on eetimes.com website (04/11/2008).
- AWR Collaborate on Advanced Radio Systems-on-Chip on EDA Geek website (04/11/2008).
- European Research Collaboration to Break Barriers for Next-generation Wireless Chips on the microwave journal (04/11/2008).
- AWR To Conduct Research For Advanced Radio Systems-On-Chip Project on rfglobalnet.com (05/11/2008).
- ICESTARS: Mathematiker an europäischem Forschungsprojekt beteiligt on the website of Wuppertaler Stadtnetz (18/11/2008).
- Drahtlose Datenübertragung wird beschleunigt - Simulationswerkzeuge dienen dem Chip-Design on Nena website.
- Schnellere drahtlose Datenübertragung on the InfoWeek website (05/11/2008).
- Drahtlose Datenübertragung wird beschleunigt on the Wallstreet Online website (05/11/2008).
- Mit "ICESTARS" unabhängig kommunizieren on media in NRW website (05/11/2008).
- Schnellere drahtlose Datenübertragung on PC Welt website (06/11/2008).
- European research collaboration to break barriers for next generation wireless chips on the innovations report website (04/11/2008).
- Breaking Barriers For Next Generation Wireless Chips on ScienceDaily (04/11/2008).
- European Research Collaboration To Break Barriers For Next Generation Wireless Chips on Wireless Design Online (05/11/2008).
- Европейские ученые разрабатывают беспроводные технологии нового поколения on Soft Mail Russia (06/11/2008).
- ICESTARS eyes next generation wireless chips on CORDIS News (05/12/2008).
- EU プロジェクト「ICESTARS」は次世代ワイヤレスチップに注目 on NEDO (NEDO is Japan's largest public R&D management organization for promoting the development of advanced industrial, environmental, new energy and energy conservation technologies).

- El proyecto "Icestars" desarrollará chips inalámbricos de bajo coste on laflecha.net (Spanish online journal about science and technology).
- ICESTARS y la próxima generación de chips inalámbricos on FECYT, the Spanish Science and Technology Foundation (11/12/2008).
- Le projet ICESTARS s'intéresse à la prochaine génération de puces sans fil on mediterranee-technologies.com.
- ICESTARS guarda alla prossima generazione di chip wireless on venetonanotech.it (09/12/2008).

A second press release about the project results is planned at the end of the project.

4.1.5 Conferences, workshops and scientific papers

The ICESTARS partners have been published their first project results at international conferences as the *SCEE 2008* (the 7th International Conference on Scientific Computing in Electrical Engineering) in Espoo, Finland, the *European Microwave Week 2009* in Rome, Italy, the *Eighth Mississippi State - UAB Conference on Differential Equations & Computational Simulations (2009)* at Mississippi State University, USA, the *ICNAAM 2009* (the 7th International Conference of Numerical Analysis and Applied Mathematics) in Rethymno, Greece and the 12th *NUMDIFF* Conference on the Numerical Solution of Differential and Differential-Algebraic Equations in Halle 2009.

- KLN: Baumanns, Selva, Tischendorf. *Consistent initialization for coupled circuit-device simulation.*(SCEE 2008)
- MAG: Schoenmaker. *Evaluation of the electromagnetic coupling between microelectronic device structures using computational electrodynamics.* (SCEE 2008)
- NXP: Harutyunyan, Schoenmaker, Schilders. *Simulation of large interconnect structures using ILU-type preconditioners.* (SCEE 2008)
- NXP: Rommes, Lenaers, Schilders. *Model order reduction for large resistance networks.* (SCEE 2008)
- FHO: Brachtendorf, Bunse-Gerstner, Lang, Lampe: *Quasiperiodic steady-state analysis of electronic circuits by a spline basis.* (SCEE 2008)
- QAG: Dautbegovic. *Wavelets in circuit simulation.*(Invited Speaker at SCEE 2008)
- WUP: Pulch. *Polynomial Chaos for the Computation of Failure Probabilities in Periodic Problems.* (SCEE 2008)
- KLN: Iwata, Takamatsu, Tischendorf. *Hybrid Analysis of Nonlinear Time-Varying Circuits Providing DAEs with at Most Index 1.* (SCEE 2008)
- NXP: Ilievski, Schilders, ter Maten. *BRAM - Backward Reduced Adjoint Method.* (SCEE 2008)
- OUL: Rahkonen. *Nonlinear distortion in differential circuits with single-ended and balanced drive.* (SCEE 2008)
- OUL: Aikio, Mäkitalo, Rahkonen. *Harmonic Load-Pull Technique Using Volterra Analysis.* (European Microwave Week 2009)
- FHO: Ashish Awasthi. *Modified Upwind Difference Scheme for Time-Dependent Singularly Perturbed Convection-Diffusion Equations on Shishkin Mesh.* (Eighth Mississippi State - UAB Conference on Differential Equations & Computational Simulations 2009)
- KLN: Matthes, Tischendorf. *Convergence analysis of a coupled circuit- and device simulation.* (ICNAAM 2009)
- KLN: Baumanns, Tischendorf. *Consistent initialization of partial-differential-algebraic equations for circuit simulation.* (NUMDIFF 2009)

Additionally, the project results are aimed to be published in high-level scientific journals. So far, ICESTARS publications include the following journal publications, preprints and theses.

- OUL: Aikio, Rahkonen. A Comprehensive Analysis of AM-AM and AM-PM Conversion in an LDMOS RF power amplifier. *IEEE Trans. Microw. Theory Tech.*, vol 57, no.2, pp. 262-270, Feb. 2009.
- NXP: Harutyunyan, Rommes, ter Maten, Schilders. Simulation of mutually coupled oscillators using nonlinear phase macromodels *IEEE Trans. on Computer-Aided Design of Integrated Circuits and Systems (TCAD)*, Vol.28-10, pp. 1456-1466, 2009.
- WUP: Pulch. Initial-boundary value problems of warped {MPDAE}s including minimisation criteria. *Mathematics and Computers in Simulation*, Vol. 79, pp. 117-132, 2008.
- NXP: Harutyunyan, Rommes. Simulation of coupled oscillators using nonlinear phase macromodels and model order reduction. *TU Eindhoven CASA-Report 2009-08.*
- NXP: Fernández Villena, Schilders, Silveira. Block oriented model order reduction of interconnected systems. *TU Eindhoven CASA-Report 2009-01.*
- NXP: Liu. Initial estimates for obtaining Periodic-Steady State solutions of free-running circuits. *MSc. Thesis Eindhoven University of Technology,* August 2009.
- OUL: Mäkitalo. Optimization of RF-amplifier's distortion using harmonic impedances. *MSc. Thesis (in Finnish), University of Oulu, Department of Electrical and Information Engineering,* 2009.

The ICESTARS project is accompanied with a series of small workshops with 2-3 partners (about once a month) and two broad workshops with all ICESTARS partners. One has been held in Hagenberg in October 2009 in connection with the *Hagenbergs Science Day*. This Hagenberg Project Workshop was scheduled as Milestone M4.2 (T0+20). Its aims were

- Public overview of activities (Public part of meeting)
- Exchange of knowhow between the partners (Public and Internal part of the meeting)

All presentations as well as the minutes have been archived at the internal project website. During the public part the following presentations were given.

- **Invited speaker**: *Uwe Knochel*, Fraunhofer EAS, Dresden, Group Manager Analog and RF Circuits: *Working areas of FraunhoferIIS/EAS focused on modelling and simulation.*
- **WP1 Time Domain Techniques**
  - Renate Winkler, WUP. *Envelope simulation by multirate methods based on wavelets*
  - Kai Bittner, WUP. *Wavelet-based simulation techniques in time domain.*
  - Ashish Awasthi, FHO. *A Mixed Time Frequency Algorithm for Circuit Simulation.*
- **WP2 Frequency Domain Techniques**
  - Timo Rahkonen, OUL. *VoHB method and it's role in PA design.*
  - (presented by) Timo Rahkonen, AWR. *Adaptivity and scalability in HB analysis*
  - Jan ter Maten, NXP (cancelled because of parallel meeting; pres. available). *Initial Conditions for Harmonic Balance.*
- **WP3 Electromagnetic Fields**
  - Wim Schoenmaker, MAG: *Construction of an electromagnetic TCAD transient solver: Interface and boundary conditions subtleties.*
  - Michael Matthes, KLN. *Time-integration methods: The DAEn solver for transient applications*

During the internal part the presentation were given devoted to exchange of knowhow between the partners

- WP1, Kai Bittner (WUP): Background & Usage wavelets algorithms
- WP2, Timo Rahkonen (OUL): Background & Usage volterra algorithms
- WP3, Michael Matthes (KLN): Background & Usage Cologne software
- Exchange of SW - definition of interfaces (Kai Bittner)

The Work Packages WP1-2-3 have received the task to prepare an IEEE paper during the test and validation phase.

The next broad workshop is planned to be held within the *ECMI (European Consortium for Mathematics in Industry) conference 2010* in order to present the project results to the scientific European community in mathematics and electrical engineering.

4.2 Dissemination plan of academic partners

All partners have presented their first research results at SCEE 2008 in Espoo, Finland. They plan further dissimination activities as explained in the following.

4.2.1 Universität zu Köln

The partner KLN plans to disseminate further research results through publications and conferences as ECMI 2010 and SCEE 2010. Additionally, the results are presented and discussed within PhD seminars at the Mathematical Institute of the University of Cologne taking place each half year. Furthermore, the developed simulations algorithms are planned to be integrated into the software platform of the numerical analysis group at the University of Cologne that is used for teaching and further applied research.

4.2.2 Bergische Universität Wuppertal

The partner WUP disseminates research results via publications in scientific journals and presentations at international conferences like GAMM, ECMI and SCEE. Furthermore, an electronic preprint series exists at WUP. Results of recent research are included in educational activities like lectures, seminars, tutorials, etc. for training students in master courses and PhD programmes.

4.2.3 Fachhochschule Oberösterreich

The partner FHO will disseminate the results from the ICESTARS project through publications and presentations in leading journals and conferences including, but not restricted to, IEE, IEEE TCAD, IEEE MTT, IEEE Circuits and Systems SIAM Journals, Acta Mathematica, Numerical Linear Algebra, Computing and Numerische Mathematik and the conferences ICCAD, DAC, DATE, and GMM-ITG. FHO has organized the *FHOOE Science Day 2009*, a yearly conference dedicated to the current research activities at the University of Applied Science.

4.2.4 University of Oulu

The partner OUL's main goals are doctoral and MSc theses, and publications in good conferences and journals. The group has written e.g. to IEEE ISCAS, European Microwave week, ECCTD and (with silicon made) to ESSCIRC conferences, as well as to IEEE TCAS, JSSC, and MTT journals, and to Springer journal of analogue integrated circuits and signal processing.

4.2.5 Helsinki University of Technology

The partner TKK plans to disseminate the project results through MSc and doctoral theses as well as publications in scientific journals and presentations in international conferences. TKK (Circuit Theory Group) has also teaching and educational activities such as lectures and research seminars to report the project results.

4.3 Dissemination plan of industrial partners

NXP, QAG, APL and MAG will actively participate in the dissemination plan, including dissemination within their respective organisations and customer base.

4.3.1 NXP

At NXP Semiconductors in Eindhoven, an annual RF simulation meeting is held, attended by NXP employees worldwide, and organized by the PDM department that participates in the ICESTARS project.

In addition at NXP regular meetings of the NMWP (Numerical Mathematics Working Party) are held. These meetings are attended by staff of NXP (mathematicians and engineers in electronics, all involved in simulation techniques), by MSc-students, PhD-students, PostDocs, and are frequently attended by guests from TU Eindhoven, TU Delft, University of Wuppertal and Magwel (Leuven). Minutes and presentations of these meetings are available.

A selected list of meetings with topics related to ICESTARS activities is given below. After the lectures, separate meetings with more detailed discussions with the external speakers were held.

- April 1, 2008:
  - Dr. Wim Schoenmaker (Magwel): *Recent Progress of the MAGWEL's Geometrical Electrodynamics based EM-TCAD software*.
  - Prof.Dr.Ir. Herbert De Gersem (KU Leuven/Kortrijk): *Anisotropic finite-element, spectral-element discretisations for models featuring geometric symmetries*.
- June 6, 2008:
  - Prof. Ferdinand Verhulst (Utrecht University): *Periodic solutions of autonomous ODEs, stability and bifurcations.*
  - Prof. Wolf-Jürgen Beyn (Bielefeld University): *The method of freezing spatio-temporal patterns in partial differential equations.*
- January 13, 2009:
  - Dr. Rob H. Bisseling (Utrecht University): *Sparse matrix partitioning by Mondriaan 2.0: applications and recent developments.*
  - Dr. Davit Harutyunyan (TU Eindhoven): *Simulation of mutually coupled oscillators using nonlinear phase macromodels.*
- May 26, 2009:
  - Prof.Dr.Ir.Drs. Hester Bijl (TU Delft); *Uncertainty quantification for unsteady flow and fluid-structure interaction.*
  - Dr. Joost Rommes (NXP Semiconductors): *Computing sensitive eigenvalues and their use in model order reduction.*

NXP plans to have additional meetings addressing topics on wavelets and periodic steady state (WP1), harmonic balance and volterra series (WP2), coupled EM and circuit simulation (WP3).

On Aug. 17, 2009, J. Liu gave a presentation at TU Eindhoven on his MSc-Thesis Initial estimates for obtaining Periodic-Steady State solutions of free-running circuits.

NXP co-organized:

- *Workshop Model Reduction for Circuit Simulation*, University of Hamburg, Oct. 30-31, 2008.
- *Multirate time integration*, SIAM-CSE (Computational Science and Engineering), MiniSymposium MS50, March 3, 2009.
- *Advanced methods for circuit simulation*, SIAM-CSE (Computational Science and Engineering), MiniSymposium MS53, March 3, 2009.
- *COMSON Autumn School on Future Developments in Model Order Reduction*, Terschelling, The Netherlands, September 21-25, 2009.

NXP is involved in the program commitees of ECMI-2010 (European Conf on Mathematics for Industry; Wuppertal, July 26-30, 2010), SCEE-2010 (Scientific Computing in Electrical Engineering; Toulouse, September 19-24, 2010), DATE-2010 (Design, Automation and Test in Europe; Dresden, March 08-12, 2010).

NXP will cooperate with the university partners in preparing presentations at conferences and publications at journals.

4.3.2 Infineon

As part of the close cooperation of the Infineon's TITAN development group with our designers, the TITAN group organizes several annual workshops on company level, which are usually very well visited by both designers and design support engineers. These events are perfect opportunity for timely dissemination of the ICESTARS results throughout our users' base.

Annual Circuit Simulation Community Meeting is a full-day event organised with the aim to bring together experts from different expert fields and Infineon business units to exchange experiences, design problems and their solutions with other colleagues. The event is geared towards the general analogue circuit simulation topics but the related topics such as fast-spice simulations or mixed analog-digital signal approaches are also discussed. In particular, current trends in (analog) circuit simulation and the solutions for current simulation issues and methodologies are discussed in resolution-oriented manner.

Another annual workshop in organisation of the group directly involved in the ICESTARS is Annual New TITAN Features Workshop. It is an interactive platform for Infineon's design supporters and designers who are particularly interested in new TITAN developments. The development engineers involved in advanced designs actively participate in this workshop and as early adopters bring the new techniques into their development teams in hands-on approach. Until now they have been very valuable route of spreading the information on improvements and new techniques available in TITAN and we expect the same in the future. In close connection to the Use plan, it is aimed that the New Features Workshop of 2011 contains a large section on a novel Wavelet analysis in TITAN.

Finally, dissemination of results outside of the company will take place together with participating universities. In particular it is expected to prepare common papers for certain conferences (e.g., SCEE 2010, etc.) in close cooperation with University of Wuppertal on the topic of wavelet-based simulation methods.

4.3.3 AWR APLAC

AWR-APLAC will present the key results in an annual AWR technical conference attended by AWR employees worldwide. The results that are available to the AWR user base will also be presented in workshops which will be arranged in several countries in EU region.

4.3.4 MAGWEL

MAGWEL has submitted a regular paper to the Design Automation Conference (DAC) for 2009. Scientific valuable results will be submitted for publication in peer-reviewed journals (IEEE Transaction on CAD). Furthermore, MAGWEL will present their key results on the company's website and promote the outcomes of the ICESTARS project in its sales activities.

5. Exploitation

The industrial partners will use ICESTARS results in their day-to-day circuit and device design activities to increase their competitive edge in the global semiconductor industry. This is to be done by increasing RF circuit and system engineering productivity both in-house and at customer side. In particular, the target is to dramatically shorten time to the market and reduce the product development costs by providing fast and accurate simulation tools that enable first-time right designs. The increased productivity will come from improving the simulation accuracy and speed, but also, largely automating these improvements, as the productivity increase does not come through experts (while they need new tools, too) but by speeding-up the work of an average engineer, who is to a large extent completely unaware of what is happening inside a design environments (s)he is using.

All industrial partners in the Consortium are fully capable of exploiting the enabling technologies that result from the ICESTARS project. In fact their participation in the project is a result of their internal plans for commercial exploitation of the results during and after the project end. On the other hand, university partners intend to use the ICESTARS results to further their educative and research tasks, more specifically to support and encourage young scientists in their efforts towards MSc. and PhD. degrees.

This alignment of a commercial vision of industrial partners and scientific interest of university partners is the win-win situation that guarantees the successful exploitation of the knowledge gained within ICESTARS even beyond the project end.

5.1 Use plan of industrial partners

5.1.1 NXP

NXP's strategy as far as simulation software is concerned centres on the development of new methodologies and tools, and to distribute these to internal customers. In addition, software from commercial vendors is constantly monitored and evaluated/benchmarked, so as to have a clear picture of the state of the art. As cost reduction is a major issue, it has recently been decided to adopt a one supplier policy, both for design and for testing. Such policies are also adopted by other major semiconductor companies.

To be at the forefront of the use of advanced RF/Mixed Signal design methods it is of the utmost importance for NXP to be competitive in the market. As far as the latter is concerned, NXP is a leader in RF/Mixed Signal. We understand the many complexities of RF/Mixed Signal design and dedicate ourselves to creating products that deliver advanced performance while simplifying design. Our portfolio covers the majority of communication and transmission systems, so it is easy to find a solution that matches the particular requirements of customers.

The output of this project is useful for enhancing the currently used virtual design environment systems by improving the efficiency of the system and adding new facilities to the system, for simulating advanced electronic structures by enabling new classes of structures to be simulated and by extending the range of the operating conditions for bringing new RF/Mixed Signal products to the market.

The main objectives of the PDM group of NXP in this area are to maintain an active knowledge on the evolution of key technologies and new concepts in this domain, to identify the most promising evolutions, to propose, develop, and evaluate innovative functions compatible with industrial and economical viability criteria, and to organize and accompany the transfer of the retained subjects to the development phase.

The interest for NXP to be a partner of the ICESTARS project is multiple:

- Feasibility of new concepts for virtual design environments
- Development of software based upon new methodologies

- Evaluation and validation of simulation results in comparison with measurements
- Increased insight in the operation of complete IC blocks
- Faster design cycles and, therefore, shortened time to market

The NXP business lines and the research centres are eager to use the developed RF design technologies in the future commercial drive. The exploitation results of the ICESTARS project will therefore get continuous attention during the project. The developed prototype will be used as a key tool for the design of commercial data transmission products, which further extends Europe's leading position in very high speed signal processing. The development and provision of efficient design support by design tools and methods, is the basis and the key for the realisation of successful products under the aspects of performance, time to market and costs. The resulting products will be the enablers for future ambient intelligence and communication networks (high bit-rate circuits, wireless and wire-line transceiver applications), for improved healthcare, communications, mobility and transport, home electronics, and car electronics. The newly developed methods extend the underlying simulation methodology with ways to take into account modern application requirements on environment and security.

The in-house analogue circuit simulator Pstar has capabilities for RF time-domain simulation (via Periodic Steady State analysis and subsequent noise analysis), Harmonic Balance frequency-domain analysis, multi-rate time integration and pole zero analysis. It offers coupling with Matlab and with Simulink for system simulation purposes. Apart from that simulation software of partner Magwel is used for electromagnetic field computations in the RF-regime.

Currently, inductive coupling effects from external fields or between various oscillators are being studied. Coupling between electromagnetic fields and circuits has become of interest (WP3). Here NXP is further interested in the combination with (nonlinear, parametric, multi-terminal) Model Order Reduction techniques. New focussing on mixed analogue digital signal analysis makes the developments on wavelet techniques and of envelope time integration techniques (WP1) of special interest. The activities in WP2 will mainly improve Pstar's capabilities for diagnosing converging problems and to make simulation more efficient.

Apart from the technical exploitation by NXP via its in-house tool Pstar and in-house design flows, commercial exploitation by our CAD tools partners, which vend circuit simulation tools, via superior capabilities of their software packages, will be advocated.

The right first time adagio is spreading fast within the company and the results of the ICESTARS project will be used to achieve these ambitious goals.

5.1.2 Infineon Technologies

For many years TITAN, an in-house analogue circuit simulator, is heavily used by design teams in all Infineon business units (Wireless Solutions, Automotive, Industrial & Multimarket, Chip card and security, etc.). Main users are designers involved in research and development of various analog and to a smaller extent digital building block of complex mobile platform solutions (transceivers/receivers for GSM/GPRS, EDGE, HSxPA, LTE, WiMax, etc.), sensors, microcontrollers, contact-based and contact-less chip card security controllers, power IC modules, etc. The competitiveness of leading-edge RF production portfolios (e.g., wireless RFIC designs, mobile phone platforms, etc.) can only be maintained if key simulation tools can enable first-time-right designs and low productions costs, i.e., high yield products. Hence, the use of these improved and new RF tools is identified as the key prerequisite for maintaining competitiveness of Infineon's products in European and worldwide RF semiconductor market.

The TITAN development team, which is directly involved in this project, has a long tradition of close cooperation with our designers, not only supporting the current design processes but also identifying possible simulation roadblocks for the upcoming technology nodes. The aim is to anticipate simulation problems and offer the solution for problems and challenges at the time when designers switch to the

smaller technology node, a change that usually brings into the spotlight (until then) unknown both quantitative and qualitative design and simulation issues.

Designers in various wireless/communication and automotive business units of Infineon AG, located in Infineon's worldwide design centres will be first beneficiaries of the knowledge generated within ICESTARS projects. The improved HB algorithms and tools developed within ICESTARS will be included in official TITAN version and driven into productive use as soon as their verification process is successfully completed. Both the ICESTARS benchmark set (see deliverable D5.2 - Test plan) and the most recent in-house design examples will be included in verification efforts.

Furthermore TITAN users involved in the mixed-signal designs are potential beneficiaries of the novel wavelet-based simulation techniques being developed within WP1. We expect that the particular property of the wavelets of flexible time-frequency resolution will enable simulation of the mixed-signal circuits with improved efficiency compared to standard analog simulation algorithms and with better accuracy than is the case with pure digital approaches. The developed prototype code will be tested in-house on the current design examples provided by this group, as to enable the best possible testing for the envisaged productive use of the newly developed wavelet-based techniques.

5.1.3 AWR APLAC

APL is part of Applied Wave Research, Inc. (AWR). AWR is a leading supplier of high-frequency electronic design automation (EDA) products for the design of wireless telecommunications, networking systems, automotive mobility systems, and a variety of other electronics-based products. AWR-APLAC Corp. is responsible for developing next generation simulation capabilities based on APLAC Simulator technology. The exploitation plan of AWR-APLAC consists of increasing the APLAC Simulator performance to help our customers increase their productivity and shorten their design cycles. Harmonic Balance and Transient analysis engines in APLAC Simulator are the basis for future simulations in AWR Design Environment. Development in these areas, as presented in ICESTAR, is crucial for success in simulating current and future RF-circuits. ICESTARS' focus is perfectly aligned with AWR-APLAC's vision and will have a direct impact on its technology roadmap. This ensures that the exploitation results will be observed and controlled to enable technology transfer from development to products.

5.1.4 MAGWEL

MAGWEL is an SME and provides tools for IC design in the full-range frequency regime (0-100 GHz). The tools are developed for analysis of the physical simulations of high-frequency responses. The company has a specific interest in offering design tools that are able to model accurately larger segments of the full IC design. In particular, functional blocks are the next level of complexity that MAGWEL will address in its next-generation products. The business plan of MAGWEL consists of expanding its product portfolio to cover tools that will enable customers to deal with design problems on the level of functional parts. MAGWEL has a seamless integration with industry-standard environments, such as Cadence's Open Access program. There is a strong interest from RFIC designers in a better, more accurate and faster layout extraction product than is available nowadays. As more than 60% of the design failure in this segment is due to parasitics and nowadays multiple silicon iterations are required to make working chips, current extractors are not adequate enough. A market field study, carried out by MAGWEL in 2007 shows that for several customers in US, Japan and Europe, there is an urgent need for better tools, and retooling will take place when a better tool comes available. If this product is available (partially based upon the ICESTARS project results), the size of the market can be estimated. The total number of Analogue, Mixed Signal and RF designers is approximately 10.000 worldwide, and the growth rate of this market segment is estimated to be 15%. This forecasting was actually overshadowed by the world-wide economical crisis but recently an up turn is detected for the customer base of MAGWEL. Whereas, research departments are forerunners is budget cuts, they are also signaling an uprising at the earliest stage. Given this insight we come to the following business case study.

Product description MAGWEL

MAGWEL has upgraded it star product “devEM” which performs combined on-/in- silicon simulation with a transient module. Whereas the original motivation as described in the DoW was to provide accurate 'back-up' modeling of device architectures up to the 60 GHz range by completion of transient simulation for combined device-circuit simulation, the transient solver has great potential to address issues at much lower frequencies. A major topic of interest is to accurately analyse the effects of substrate currents due to device switching and latch-up. A modeling of the substrate as a lowly-conductive layer ignores the presence of capacitivly coupled junctions and this gap can be bridged by using the newly developed transient modules from the ICESTARS project. Another important development for the MAGWEL product is it extension with circuit simulation. However, contrary to the 'conventional' mixed-mode simulations, in which the field solver provides a 'client' process for the circuit simulator (master process), the MAGWEL tool allows for insertion of hundreds of ports (contacts) to which elementary circuit elements can be attached. In many interesting applications, the circuit elements are clones of an active device. The simulator is then able to perform an in-depth and accurate modeling of the current flow in power MOS devices. This product branch is now already an important pillar of the MAGWEL business and its development is clearly rooted in the WP3 activities of ICESTARS.

Business case study

Our financial projections for the first five years after completion of the project are given in Fig.1. We assume that the product will be launched in 2011 after the completion of the project. Before product launch we plan at least 3 beta test cycles in 2011 with motivated customers some of which will be participants in the ICESTARS project. In that year we project to sell 6 licenses of the new product primarily to our beta customers. After the first year we project a growth of the number of licenses sold of 50% per year. We project an average license price per year of 50,000 EURO in the first year and an increase of 5% per year in the following years. This starting price and the rate of increase is based on our experience with our current simulation products. Rate increase is justified because the product will gain traction and brand recognition over time.

Year	1	2	3	4	5
Price per year	50	55	60	65	170
New Licenses	6	9	12	18	23
Cumulative licenses	6	15	27	45	68
Revenue (1,000 EUR)	300	500	725	1175	1600
Cumulative Revenue	300	800	1525	2700	4325
Employees	3	4	6	7	8
Expenses	400	500	800	900	1000
Cumulative expenses	500	1000	1800	2700	3700

Fig.1: Financial projections for the ICESTARS solver for the first 5 years after product launch in 2011

Number of licenses sold per year and the cumulative number of licenses sold is shown in Fig. 2. Product revenue in a given year is calculated as the cumulative number of licenses sold multiplied by the license price per year using a time based license (TBL) model. This leads to a cumulative product

income of 9 MEUR in 5 years. We expect the product life cycle to be at least 10 years. So the cumulative product income over the total product life cycle will be at least 15 MEUR.

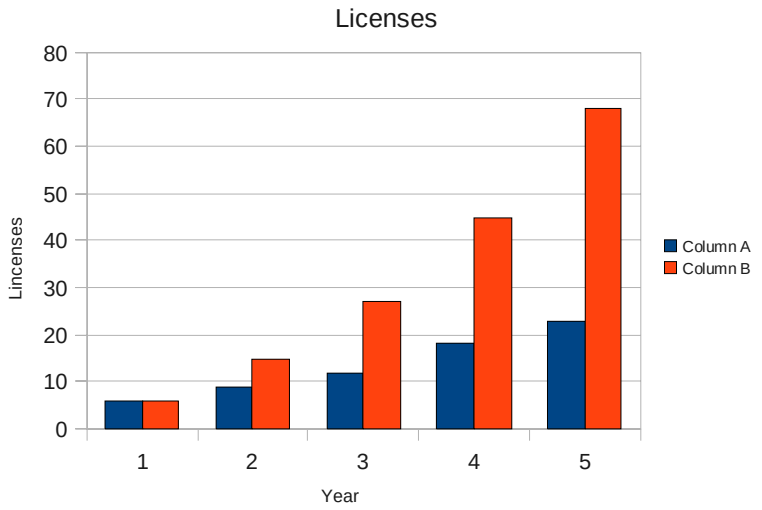

Fig. 2: Annual number (column A) and cumulative number of product licenses (column B) sold.

5.2 Use plan of academic partners

5.2.1 Universität zu Köln

The Mathematical Institute of the University of Cologne provides lectures and seminars about the numerical simulation of integrated circuits and semiconductor elements to diploma, master and PhD students. It is planned to include the results of the project in terms of new methods and algorithms into the courses. Furthermore, PhD students are directly involved into the project. They profit from the close cooperation between academia and industry. It includes to learn how to use and contribute to commercial simulator packages from the industrial partners. Furthermore, new mathematical methods and algorithms in the field of EM and circuit simulation will be tested directly by industrial RF circuit examples.

5.2.2 Bergische Universität Wuppertal

WUP will use the results as an input for further research, i.e. possible PhD positions and Post-Doc activities. In addition, selected parts will enter the teaching of the group, i.e. lectures, seminars, etc. on advanced topics for master and PhD students. The results of the project allow for further intensive cooperation between academia and industry.

5.2.3 Fachhochschule Oberösterreich

FHO will use the results for further R&D in the field of transceiver designs in the K/Ku bands. Furthermore, this project will foster the leading position in the field of multi-rate circuit simulation. The results will be disseminated via publications in leading journals in this field, in workshops and in special sessions of international conferences.

5.2.4 University of Oulu

OUL, Department of Electrical Engineering is an educational and research institution, with main interest in public research and reporting the results as journal papers and MSc and doctoral theses. The group does research on high-efficiency, high-linearity RF transmitters, and this research adds the knowledge of the design methods of these.

5.2.5 Helsinki University of Technology

TKK (Circuit Theory Group) provides lectures ranging from fundamental circuit theory, i.e., basic courses for MSc students, to advanced courses, both theoretical and numerical, to MSc and PhD students. Having access to APLAC Circuit Simulator and working in co-operation with AWR APLAC gives us the opportunity to use the project results both in educational and teaching areas as well as in further research activities.

6. Intellectual Property

A Consortium Agreement (CA), which is based on the EICTA model (dated 17 January 2007), is negotiated between all partners before the start of the project, settling among other things the internal organisation of the consortium, reflecting what has been described about the project management structure of ICESTARS in Section B2.1 of Annex I – "Description of Work". The agreement also provides additional rules for dissemination to ensure smooth dissemination of the results. This document is entirely in agreement with these rules. Settlements of internal disputes and of course Intellectual Property (IP) arrangements are also part of the Consortium Agreement.

The IP terms during and afterwards the cooperation of ICESTARS are based on royalty free terms and conditions if these terms may reasonably be expected. If not, fair and reasonable conditions may apply. The IP terms of ICESTARS are consolidated before the Model Grant Agreement with the Commission was signed.